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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,833	01/16/2002	Jeffrey Craig	SANDP007	1181

66785 7590 12/21/2006

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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,833	CRAIG ET AL.	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☒ This action is **FINAL**. 2b) This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-17,20-34,36-38,41-43,45 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7,9-17 and 20* is/are allowed.

6)☒ Claim(s) *1-5,21-34,36-38,41-43,45 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Final Rejection

Response to Arguments

1. The Remarks on page 12 pertaining to the rejection of Claim 30 under 35 USC 112 still stand. Though the Applicant discusses an amendment to claim 29 in order to overcome the 35 USC 112 rejection, claim 29 itself has not been amended.

2. Applicant's arguments, see the Applicant's remarks on pages 12 and 13, filed November 22, 2006, with respect to the 35 USC 102 rejection of claim 6 has been fully considered and are persuasive. The prior art rejection of claim 6 has been withdrawn.

3. The Examiner respectfully disagrees with the Applicant's arguments on pages 13 and 14 of the Remarks concerning the 35 USC 102 rejection of claim 34 pertaining to a difference between "incrementing" and "decrementing". Though claim 34 has been amended to remove a means-plus-function limitation with respect to a counter being decremented, it is still interpreted that the section in MPEP 2184(II)(A) is still applicable. The rationale behind the equivalence of incrementing a counter and decrementing a counter in order to obtain the same result is held by the Examiner as has been previously discussed in past Office Actions. Further, the Applicant's invention as disclosed in the Specification on page 15 in lines 12-14 describes an equivalent embodiment of the claimed invention where a counter is being incremented instead of decremented. The preceding response also applies to claim 2.

4. The Examiner respectfully disagrees with the Applicant's arguments on page 14 of the Remarks concerning the 35 USC 102 rejection of claim 41 pertaining to saving an indication related to an unreliable system. Moshayedi discloses that preemptive action is taken in order to avert failure of a storage system (paragraph [0056]). It is interpreted that the storing of information is an indication of an unreliable state in itself. The generated indication may be interpreted as the information stored. The generated indication may also be interpreted as the copied data stored on another device. It is also interpreted that an alert message may act as an indication, and that the alert message is inherently stored somewhere in a computer system.

The Examiner interprets the claimed saving of an indication as not being a defining feature of the novelty of the Applicant's invention, and not specific enough as to overcome the applied prior art Moshayedi.

5. The Examiner respectfully disagrees with the Applicant's arguments on pages 14 and 15 of the Remarks concerning the 35 USC 103 rejection of claims 1-5 pertaining to a lack of motivation to combine the teaching of the applied prior art references Auclair et al. and Moshayedi. It is interpreted that the desirability of implementing the invention of Auclair et al. is to increase the fault tolerance of a storage system that conserves power and accesses memory quickly. The inclusion of ECC with stored data is interpreted as increasing the fault tolerance of a storage system and the data stored therein. The language "a usual ECC is then calculated", as disclosed in column 7 lines 22-23 of Auclair et al., implies that it is well-known in the art to include ECC with data stored on a storage device. A person skilled in the art at the time the

invention was made would have found it desirable to increase the overall fault tolerance of a storage system by including such ECC, and reducing the overall cost and resources necessary to implement as storage system, by combining Auclair et al. and Moshayedi. Further motivation to combine is discussed below in the claim rejections to follow.

6. The Examiner respectfully disagrees with the Applicant's arguments on page 15 of the Remarks concerning the 35 USC 103 rejection of claim 15 pertaining to a lack of desirability to combine Auclair et al. and Moshayedi. As discussed previously, and in the claim rejections to follow, it is interpreted that the Examiner has presented a desirable suggestion to combine the references.

7. The Examiner respectfully disagrees with the Applicant's arguments on pages 15 and 16 of the Remarks concerning the 35 USC 103 rejections of claims 45 and 46 pertaining to the taking of Official Notice with respect to a variety of memory devices. In addition to it being well-known in the art that a variety of memory cards as disclosed in the limitations of claims 45 and 46, one skilled in the art would have been motivated to include a variety of storage media in the invention of Moshayedi because a variety of formats of storage media allows for a variety of different applications based upon considerations such as cost, power, and storage implementation.

8. The Examiner respectfully disagrees with the Applicant's arguments on pages 16 and 17 of the Remarks concerning the 35 USC 103 rejection of claims 21-31 pertaining to the lack of

motivation for combining the Kozakai and Moshayedi references. The Examiner interprets that the motivation is related to and directed towards the integrating of a memory and a controller on the same chip, as discussed in the Kozakai reference, and referenced in the rejection of claims 21-31 to follow, and is sufficient to combine the two references. The exclusion of a program memory is not interpreted as being relevant to a motivation to combine the references.

9. The Examiner respectfully disagrees with the Applicant's arguments on page 17 of the Remarks concerning the rejection of claim 28 pertaining to the combination of Kozakai and Moshayedi failing to teach of a unit of erase is a sector. Paragraph [0039] of Moshayedi teaches that a memory area that may be determined to be faulty is made up of sectors. Column 5 lines 6-18 of Kozakai teaches that a sector may be defective. It is interpreted that the two references have been appropriately combined and that the Examiner has presented sufficient motivation for such combination in this and previous Office Actions.

10. The Examiner respectfully disagrees with the Applicant's arguments on pages 17 and 18 regarding the 35 USC 103 rejection of claims 32 and 33 pertaining to a lack of motivation to combine the Shaberman reference with the Moshayedi and Kozakai references. It is interpreted that interchangeability of memory cards allows for a broader use of applications for a memory card device. The interleaving allowing for the interchangeability of memory cards (column 3 lines 26-29) as taught by Shaberman et al. also offers as a benefit to a user the ability to access data, regardless of the type of data, on a memory card at very fast speeds (column 1 line 67 through column 2 line 3). The discussed reasons for motivations are interpreted as adequate in

order to combine the three references. Further, it is well-known in the art that a host computer system may play audio and display video, and that such data may be stored in and accessed from a memory device.

Claim Objections

11. Claim 6 is objected to because of the following informalities: line 12 contains a second "," after "reassigned,". Appropriate correction is required.

12. Claim 32 is objected to because of the following informalities: line 2 contains inappropriate commas between "one of" and "audio information", and "audio information" and "an wireless". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claim 30 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Claim 21, of which claim 30 is ultimately dependent upon, discloses in line 3 the limitation "a memory system on a first chip". Claim 30 discloses a memory card, which is

defined in claim 29 as "the memory system", as being selected from a group comprising various memory cards. The Examiner interprets a memory "card" as not being able to be "on" a "chip", but rather a memory "card" itself is comprised of one or more "chips".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 34, 36-38, and 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Moshayedi (U.S. PGPub 2002/0091965).

As in claim 34, Moshayedi discloses a memory system for storing information, the memory system comprising:

a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*;

means for storing a threshold *(paragraphs [0036] and [0053])*;

means for reassigning a spare unit of erase of the plurality of spare units of erase *(paragraphs [0041]-[0043])*;

a counter *(Abstract, paragraphs [0016] and [0050], page 7 claim 36)*, the counter being arranged to be decremented each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050])*;

means for storing the counter *(paragraphs [0036] and [0050])*;

means for comparing the counter to the threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are yet to be reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-[0055])*; and

means for generating an indication when comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is substantially near a failure condition *(paragraphs [0053]-[0055])*.

As in claim 36, Moshayedi discloses the means for comparing the counter to the threshold value include means for determining when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 37, Moshayedi discloses the first result is arranged to indicate that the value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0056])*.

As in claim 38, Moshayedi discloses means for attempting to write data to a first unit of erase *(paragraphs [0040]-[0042])*;

means for determining when the first unit of erase is worn, wherein the means for reassigning the unit of erase include means for reassigning a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase when it is determined that the first unit of erase is worn *(paragraphs [0041]-[0043])*, and wherein the means for updating the counter include means for updating the counter to indicate that the first spare unit of erase is reassigned *(paragraph [0050], page 7 claim 36)*; and

means for writing the data to the reassigned first spare unit of erase *(paragraph [0042])*.

As in claim 41, Moshayedi discloses a method for determining a status associated with a non-volatile memory system *(paragraphs [0007] and [0034])*, the non-volatile memory system including a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*, the method comprising:

automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0055])*;

generating an indication when it is determined that the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(Abstract, paragraph [0056], page 7 claim 35)*, wherein the indication is arranged to indicate that the non-volatile memory system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0056])*;

saving the indication *(paragraph [0056], where the indication is the updating of information)*;

wherein automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable includes:

updating a counter, the counter being arranged to be updated each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050])*; and

comparing the counter to a threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are not to be reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-[0055])*.

As in claim 42, Moshayedi discloses generating the indication when it is determined the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable includes:

determining when comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is nearing the condition which renders the non-volatile memory systems as being substantially unreliable when comparing the counter to the threshold value yields the first result *(paragraphs [0053]-[0055])*.

As in claim 43, Moshayedi discloses the condition which renders the non-volatile memory systems as being substantially unreliable when comparing the counter to the threshold value yields the first result is one of an end-of-life condition and a fault condition *(Abstract, paragraphs [0053]-[0056])*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Auclair et al. (U.S. Patent No. 6,016,530).

As in claim 1, Moshayedi teaches a method for determining a status associated with a memory system, the memory system including a plurality of spare units of erase, the method comprising:

receiving user data for storage in the memory system *(paragraph [0035])*;

storing the user data in a first unit of erase if the first unit of erase is not unreliable *(paragraph [0040])*;

reassigning a first spare unit of erase of the plurality of spare units of erase in the reassigned first spare unit of erase if the first unit of erase is unreliable *(paragraphs [0041]-[0042])*;

updating a counter each time a spare unit of erase of the plurality of spare units of erase is reassigned *(page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050] lines 7-9, page 7 claims 35 and 36)*;

comparing the counter to a threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are yet to be reassigned in order for the memory system to be considered as reliable *(paragraphs [0053]-[0054], page 7 claim 35)*; and

generating an indication when comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is substantially near a failure condition *(Abstract, paragraph [0056], page 7 claim 35, where an action taken is interpreted as a first result)*.

However, Moshayedi fails to teach of error correction codes. Auclair et al. teaches of calculating an error correction code from the user data and storing the error correction code together with the user data in units of erase *(column 7 lines 18-22)*.

It would have been obvious to have included the error correction codes as taught by Auclair et al. in the invention of Moshayedi. This would have been obvious because the invention of Auclair et al. offers a fault tolerant fast-access, low power memory storage *(column*

1 lines 34-60). Further, it is well-known in the art to include ECC data in conjunction with user data for fault tolerance when saving such data to a memory device.

As in claim 2, Moshayedi discloses updating the counter includes decrementing the counter each time a spare unit of erase of the plurality of spare units of erase is reassigned *(Abstract, paragraph [0016], page 7 claim 36)*.

As in claim 3, Moshayedi discloses comparing the counter to the threshold value includes determining when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 4, Moshayedi discloses the first result is arranged to indicate that the value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0056])*.

As in claim 5, Moshayedi discloses attempting to write data to a first unit of erase *(paragraphs [0040]-[0042])*;

determining when the first unit of erase is worn *(paragraphs [0041]-[0042])*;

reassigning a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase when it is determined that the first unit of erase is worn *(paragraphs [0041]-[0043])*, wherein updating the counter includes updating the counter to indicate that the first spare unit of erase is reassigned *(paragraph [0050], page 7 claim 36)*; and

writing the data to the reassigned first spare unit of erase *(paragraph [0042])*.

* * *

16. Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Official Notice.

As in claim 45, Moshayedi teaches a non-volatile memory system for storing information *(paragraphs [0007] and [0034])*, the non-volatile memory system comprising:

a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*;

means for automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0055])*; and

means for generating an indication when it is determined that the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(Abstract, paragraph [0056], page 7 claim 35)*, wherein the indication is arranged to indicate that the non-volatile memory system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0056])*;

wherein the non-volatile memory is one of a memory card *(paragraphs [0007] and [0034])*;

wherein the means for automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable include:

means for updating a counter, the counter being arranged to be updated each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050])*; and

comparing the counter to a threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are not to be reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-[0055])*.

However, Moshayedi fails to teach the non-volatile memory is one of a PC card, a CompactFlash card, a MultiMedia card, a Smart Media card, a Memory Stick card, and a Secure Digital card *(paragraphs [0007] and [0034])*. The Examiner takes Official Notice that one of ordinary skill in the art would have thought it obvious to have implemented any one of the above-mentioned types of memory cards in the invention of Moshayedi. This would have been obvious because the above-mentioned memory cards are well-known in the art.

As in claim 46, Moshayedi teaches the means for generating the indication when it is determined the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable include:

means for determining when the means for comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is nearing the condition which renders the non-volatile memory systems as being substantially

unreliable when the means for comparing the counter to the threshold value yields the first result *(paragraphs [0053]-[0055])*.

* * *

17. Claims 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Kozakai et al. (U.S. Patent No. 6,643,725).

As in claim 21, Moshayedi teaches a system, comprising:

a host system *(Figs. 1A and 1B; paragraphs [0032]-[0037])*;

a memory system, the memory system interfacing with the host system *(Figs. 1A and 1B; paragraphs [0032]-[0037])*, the memory system including,

a plurality of units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*,

a plurality of spare units of erase *(Fig. 2; paragraphs [0041]-[0042] and [0048])*, and

a first storage element, the first storage element being containing a counter and a threshold *(paragraphs [0050] and [0053])*, the counter indicating a number of spare units of erase included in the plurality of spare units of erase *(paragraph [0050])*, the threshold indicating a number of spare units of erase which are not to be reassigned *(paragraph [0053])*; and

a controller, the controller updating the counter each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase included in the plurality of spare

units of erase which have yet to be reassigned *(paragraph [0050])*, the controller comparing the counter to the threshold value to determine if the memory system is substantially near an end-of-life condition *(paragraphs [0053]-[0055])*.

However, Moshayedi fails to teach of the memory system being on a first chip. Kozakai et al. teaches of a memory system on a single chip *(Fig. 1; column 2 line 65 and column 3 line 55 through column 4 line 2)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the single chip memory system as taught by Kozakai et al. in the invention of Moshayedi. This would have been obvious because the invention of Kozakai et al. conserves and utilizes space efficiently in a memory system *(column 1 lines 45-55 and column 2 line 65 through column 3 line 2)*. Further, a single-chip memory system operates faster and consumes less power than a multi-chip configuration *(column 12 lines 43-46)*.

As in claim 22, Moshayedi discloses the controller determines when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 23, Moshayedi discloses when it is determined that the value of the counter is less than or equal to the threshold value, the controller generates an indication that the memory system is substantially near the condition *(Abstract, paragraph [0056])*.

As in claim 24, Moshayedi discloses the host system is arranged to request that data be written to the memory system, and the controller is included in the memory system, the

controller further being arranged to attempt to write the data to a first unit of erase included in the plurality of units of erase in response to the request *(paragraphs [0040]-[0042])*, and to determine if the first unit of erase is worn *(paragraphs [0041]-[0042])*.

As in claim 25, Moshayedi discloses when it is determined that the first unit of erase is worn, the controller reassigns a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase and writes the data into the reassigned first spare unit of erase *(paragraphs [0042] and [0050], page 7 claim 36)*.

As in claim 26, Moshayedi discloses the host system is arranged to request that data be written to the memory system, and the controller is included in the memory system, the controller further being arranged to attempt to write the data to a first unit of erase included in the plurality of units of erase in response to the request, and to determine if the first unit of erase is defective *(paragraphs [0040]-[0042])*.

As in claim 27, Moshayedi discloses when it is determined that the first unit of erase is defective, the controller reassigns a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase and writes the data into the reassigned first spare unit of erase *(paragraphs [0041]-[0043])*.

As in claim 28, Moshayedi teaches an individual one of the plurality of units of erase is a memory location, and an individual one of the plurality of spare units of erase is a spare memory

location *(Fig. 2; paragraph [0039])*. Kozakai et al. teaches of a memory location in a flash memory being a sector *(column 5 lines 6-18)*.

As in claim 29, Moshayedi discloses the memory system is a memory card *(paragraphs [0007] and [0034])*.

As in claim 30, Kozakai et al. discloses the memory card is one selected from the group consisting of a PC card, a CompactFlash card, a MultiMedia card, a Smart Media card, a Memory Stick card, and a Secure Digital card *(column 1 lines 29-21, where a PCMCIA-ATA type flash memory card is interpreted as a PC card)*.

As in claim 31, Moshayedi discloses the host system is arranged to capture information and to attempt to store the information in the memory system *(paragraph [0032])*.

* * *

18. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Kozakai et al., further in view of Shaberman et al. (U.S. Patent No. 5,761,732).

As in claim 32, the combined invention of Moshayedi and Kozakai et al. teaches the limitations of claim 31. However, the combined invention of Moshayedi and Kozakai et al. fails

to teach information is one of audio information and wireless information. Shaberman et al. teaches information is one of audio and wireless information *(column 1 lines 10-18, where it is inherent that information stored in a cellular phone and audio recorder is at least one of audio information and wireless information)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the information as taught by Shaberman et al. in the combined invention of Moshayedi and Kozakai et al. This would have been obvious because the invention of Shaberman et al. allows for interchangeability of memory cards in differing systems *(column 2 lines 11-16)*.

As in claim 33, Shaberman et al. teaches the host system is one of a cellular communications device, an audio player, and a video player *(column 1 lines 10-18)*.

Allowable Subject Matter

19. Claims 6, 7, 9-17, and 20 are allowed.

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
12/18/2006

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